**Title:- Implementation of 4 :1 Multiplexer using Data flow modelling**

**Code**

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-- Company:

-- Engineer:

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-- Create Date: 15:05:22 09/24/2015

-- Design Name:

-- Module Name: mux4to1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity mux4to1 is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

c : in STD\_LOGIC;

d : in STD\_LOGIC;

s1 : in STD\_LOGIC;

s0 : in STD\_LOGIC;

y : out STD\_LOGIC);

end mux4to1;

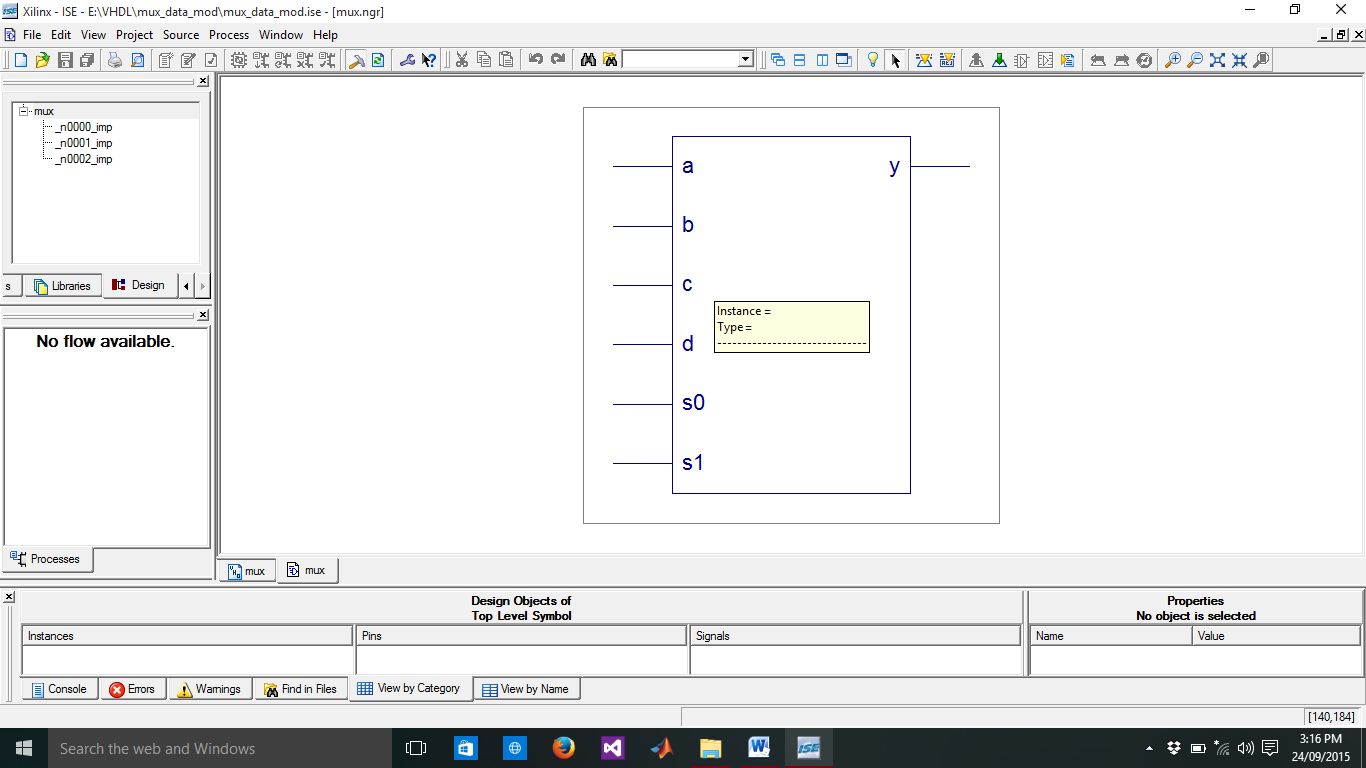
architecture Behavioral of mux4to1 is

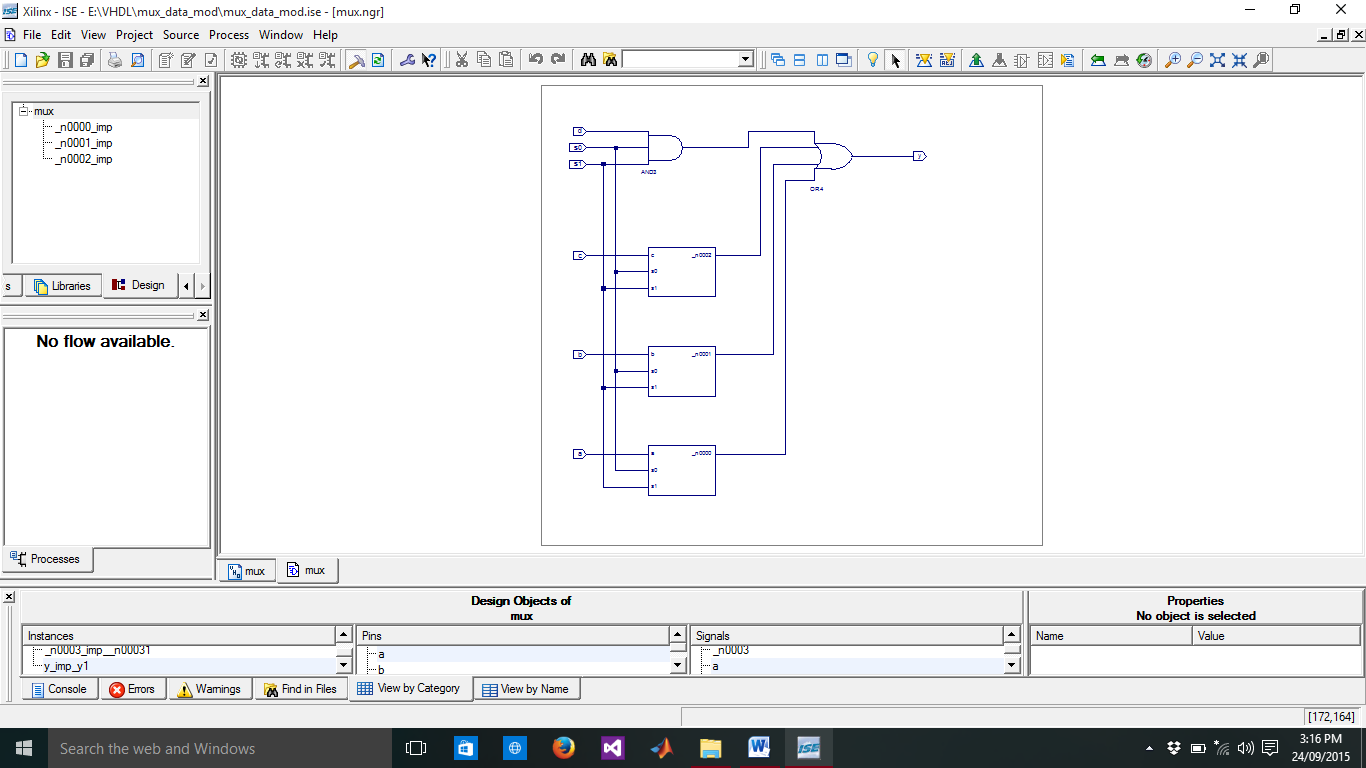
begin

y<= (not s1 and not s0 and a)or (not s1 and s0 and b)or (s1 and not s0 and c) or ( s1 and s0 and d);

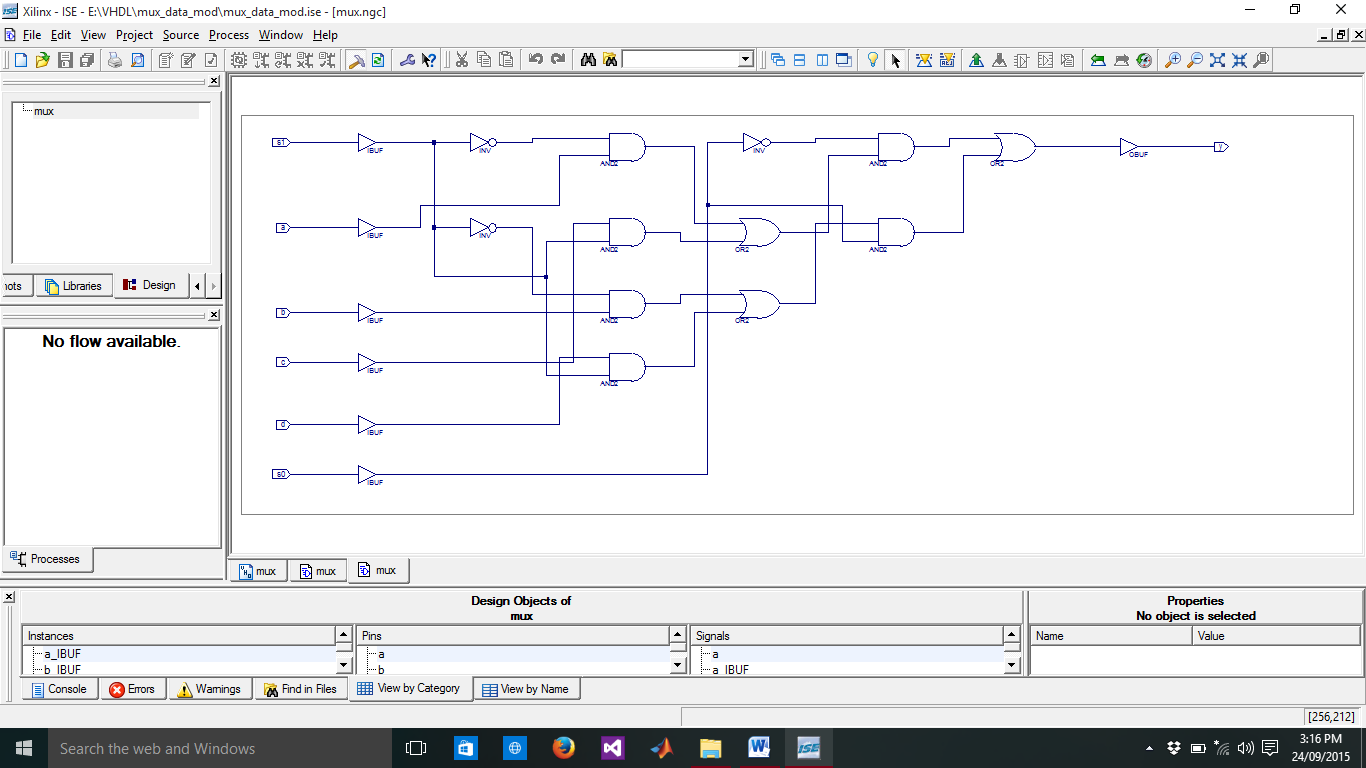
end Behavioral;

**RTL Schematic**

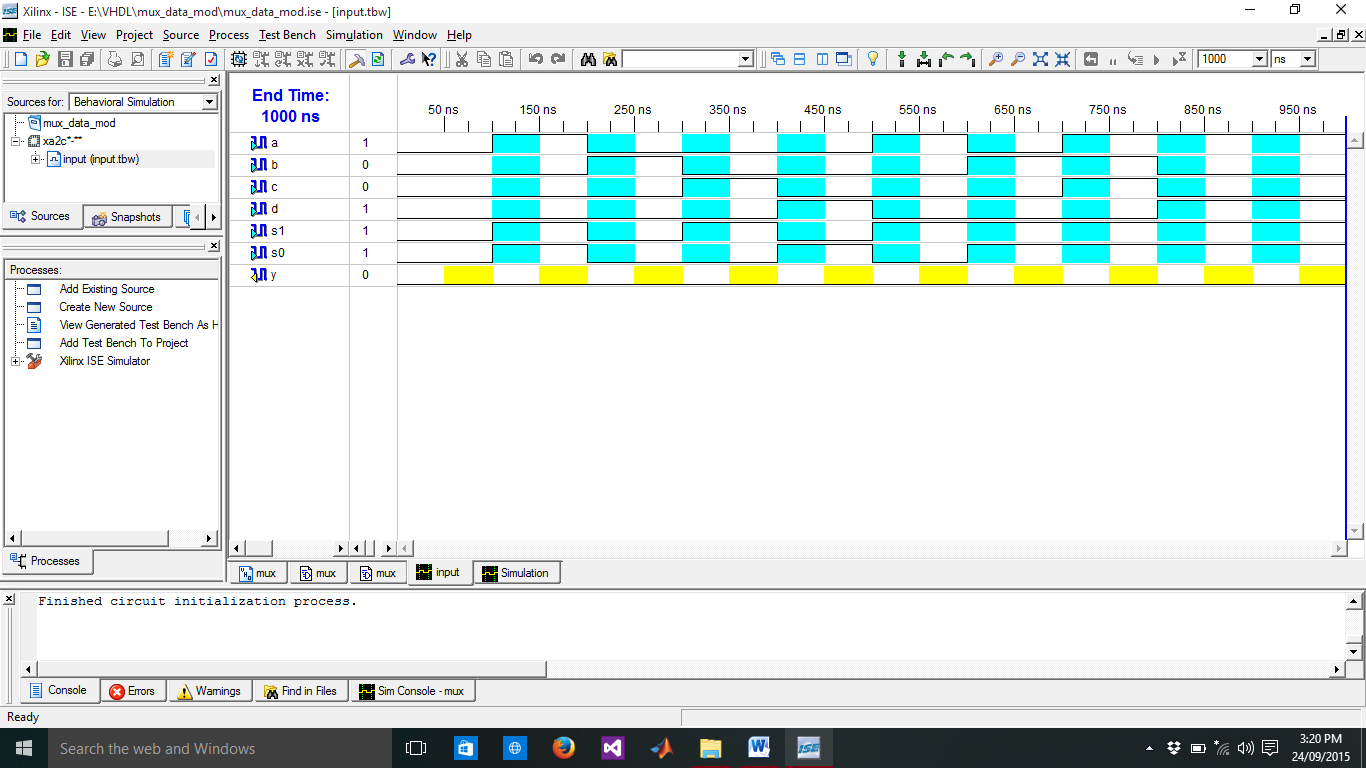




**Technology Schematic**



**Input Waveforms**



**Output Waveforms**

